UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

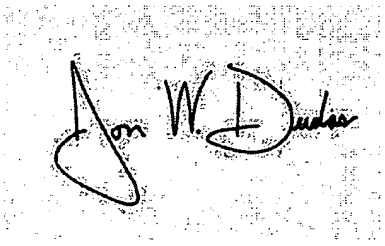
PATENT NO. : 7,120,810 B2
APPLICATION NO. : 10/784846
DATED : October 10, 2006
INVENTOR(S) : Maher et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At patent column 6, line 17, please correct to read --FIG. 1 illustrates a block diagram of a computer system.--;
At patent column 6, line 34, please delete "operations a for" and insert --operations for--;
At patent column 7, line 15, please delete "spins" and insert --pins--;
At patent column 8, line 17, please delete "will not e result" and insert --will not result--;
At patent column 8, line 17, please delete "in the e power" and insert --in the power--;
At patent column 8, line 66, please delete "thereby e suspending" and insert --thereby suspending--;
At patent column 9, line 21, please delete "the cache e memory" and insert --the cache memory--;

Signed and Sealed this

Twenty-seventh Day of February, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office